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10/5/2007

Claimed Foreign Priority Date: 2/1/00 (JPX)

Applicant(s): Koyama et al. (Kato)

Examiner: Howard Weiss

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Initially, and with respect to Claims 1, 77 to 80 and 122 to 125, note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not

patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases as the above case law makes clear.

3. Claims 1, 77, 79 to 81, 83, 84, 87, 89, 90, 93, 95 to 98, 100 to 103, 106, 108 to 111, 113 to 116 and 122 to 149 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document) and Tsutsumi (U.S. Patent No. 5,844,274).

Yamazaki et al. show most aspects of the instant invention (e.g. Figures 1 to 8) including:

- a memory cell array with memory cells formed in a n x m matrix with X-address **101** and Y-address **102** decoders electrically connected to signal lines **Cnn,Dnn, Amm,Bmm**
- each cell containing a memory thin film transistor (MTFT) **Tr1** and a switching thin film transistor (STFT) **Tr2**
- said MTFT including:
 - a first semiconductor active layer **202** formed on an insulating substrate **201**, having a first thickness **d1** and comprising a channel forming region **205**
 - a first insulating film **211**, a conductive layer (i.e. floating gate electrode) **213** adjacent to the first semiconductive active layer and used to trap electrons, a second insulating film **214** of an oxide and a control gate electrode **215**

- a wiring **825** for connecting the control gate to a first single line **809**
- said STFT including:
 - a second semiconductor active layer **206** formed on an insulating substrate **201** and having a second thickness **d2**
 - a gate insulating layer **212** and a gate electrode **217**
 - a second signal line **810** connected to said gate electrode
- where in **d1** is thinner (i.e. smaller) than **d2** (Paragraphs 0058 and 0059)

Yamazaki et al. does not show the floating gate comprising silicon with one conductivity, the control gate comprising a laminate of three films: TaN/W/WN and each film comprising the inert element xenon.

Tsutsumi teaches (e.g. Column 17 Lines 14 to 20) it is common, and therefore obvious, to form gate electrodes of layers comprising TaN/W/WN. It would have been obvious to a person of ordinary skill in the art at the time of invention to form gate electrodes of layers comprising TaN/W/WN as taught by Tsutsumi in the device of Yamazaki et al. since it is common in the art to do so. Also, it is common to use silicon with one conductivity (e.g. doped polysilicon) as floating gate material.

As to the grounds of rejection under "Product-by-Process", how the first and second films are formed, either by sputtering using an inert gas or by some other means, pertains to intermediate process steps which does not affect the final device structure. See MPEP § 2113 which discusses the handling of "product by process" limitations.

4. Claims 117, 118, 120, 121 and 150 to 153 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Tsutsumi, as applied to Claim 1 above, and further in view Akbar (U.S. Patent No. 5,656,845).

Yamazaki et al. and Tsutsumi show most aspects of the instant invention (Paragraph 4) except for the first and second semiconductor layer in a common semiconductor island. Akbar teaches (e.g. Figures 1 and 8 to 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al. and Tsutsumi to provide memory cells with improved performance and reliability.

5. Claims 78, 82, 88, 94, 99, 105 and 112 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Tsutsumi, as applied to Claim 1 above, and further in view of Koyama (U.S. Patent No. 5,793,344).

Yamazaki et al. and Tsutsumi show most aspects of the instant invention (Paragraph 4) except for the semiconductor device comprising a pixel portion over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate and a gate wiring driver circuit for driving the pixel portion over the substrate for controlling the non-volatile memory circuit all part of an LCD of a video camera. Koyama teach (Paragraph 3) to use the memory device with the listed devices to produce a high quality display device (Column 7 Lines 55 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to use the memory device of Yamazaki et al. and Tsutsumi with the listed devices of Koyama to produce a high quality display device.

6. Claim 119 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., Tsutsumi and Koyama, as applied to Claim 78 above, and further in view of Akbar.

Yamazaki et al., Tsutsumi and Koyama show most aspects of the instant invention (Paragraph 6) except for the first and second semiconductor layer in a common semiconductor island. Akbar teaches (e.g. Figures 1 and 8 to 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) 122 to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al., Tsutsumi and Koyama to provide memory cells with improved performance and reliability.

Response to Arguments

7. Applicant's arguments filed 3/21/2008 have been fully considered but they are not persuasive. The Applicants state that rejection of the pending claims should not be maintained since the prior art do explicitly form the first and second films using sputtering with an inert gas as a sputtering gas and the "product-by-product" argument does not apply since the sputtering prevents pealing of the layers. However, the Examiner maintains that forming the films using sputtering or any other technique is a "product-by-product" limitation and does not affect the final device structure. The argument that the prevention of pealing of the layer does not apply since this limitation is not explicitly stated and the prior art does not say that pealing is a problem. The Applicants have not satisfactorily established the limitation of forming said layers using sputtering with an inert sputtering gas is structurally different from the structure of the combination of the prior art as stated in the rejections above. The use of sputtering or any other means to form the films is still a "product-by-process" limitation and does not have any weight in evaluation the patentability of the instant invention. For these reasons and those stated in the rejections above, the pending claims remain rejected.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 7:00 AM to 3:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Howard.Weiss@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on **(571) 272-1705**.
11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

12. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/326, 347; 365/ 185.05	thru 6/10/2008
Other Documentation: none	
Electronic Database(s): EAST	thru 6/10/2008

HW/hw
14 June 2008

/Howard Weiss/
Primary Examiner
Art Unit 2814